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| 10/807,545 | 03/24/2004 | Mitsuaki Osame | 12732-223001 / US7068/714 | 3777 |
| 26171 7590 01/22/2010 FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022 | | | EXAMINER BECK, ALEXANDER S | |
| | | | ART UNIT 2629 | PAPER NUMBER |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| | | | |
|------------------------------|--------------------------------------|-------------------------------------|--|
| Office Action Summary | Application No. 10/807,545 | Applicant(s) OSAME ET AL. | |
| | Examiner Alexander S. Beck | Art Unit 2629 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 November 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3, 15, 17, 19, 25, 28, 32 and 34-60 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3, 15, 17, 19, 25, 28, 32 and 34-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 November 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendment filed November 2, 2009 (“Amend.”), in which: claims 1, 2, 4-14, 16, 18, 20-24, 26, 27, 29-31 and 33 are cancelled; claim is amended; new claims 34-60 are added; and the rejections of the claims are traversed. Claims 3, 15, 17, 19, 25, 28, 32 and 34-60 are currently pending and an Office action on the merits follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 36-39, 43, 46, 50 and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Pub. No. 2001/0002703 by Koyama (“Koyama”).

As to claim 36, Koyama discloses a light-emitting device comprising:

a pixel (*see* Koyama, 104; Fig. 3) (*see also* Koyama, ¶ [0115]) comprising:

a light-emitting element (*see* Koyama, 111; Fig. 3) (*see also* Koyama, ¶ [0116]),

a first transistor (*see* Koyama, 112; Fig. 3) for determining a value of a current flowing to the light-emitting element (*see* Koyama, ¶ [0117]), and

a second transistor (*see* Koyama, 109; Fig. 3) for determining a light emission or non light emission of the light-emitting element depending on a

video signal input through a signal line (*see* Koyama, 107; Fig. 3) (*see also* Koyama, ¶ [0117]),

wherein the light-emitting element, the first transistor, and the second transistor are connected in series between a first power line (*see* Koyama, 110; Fig. 3) and a counter electrode of the light-emitting element, and

wherein a source of the first transistor (*see* Koyama, 112; Fig. 3) is connected to the first power line (*see* Koyama, 110; Fig. 3) and a gate electrode of the first transistor (*see* Koyama, 112; Fig. 3) is connected to a second power line (*see* Koyama, 113; Fig. 3) so that a voltage between the gate electrode and the source of the first transistor is constantly fixed (*see* Koyama, ¶¶ [0132] and [139]).

As to claim 37, most of the limitations have been addressed in the discussion of claim 36 above, with the exception of: a third transistor (*see* Koyama, 105; Fig. 3) for controlling an input of the video signal (*see* Koyama, ¶ [0116]), of which Koyama discloses.

As to claim 38, all of the claim limitations have already been addressed in the discussion of claim 36 above. Examiner respectfully submits that the "light-emitting element" addressed in claim 36 corresponds to the "pixel electrode" in claim 38.

As to claims 39 and 46, Koyama discloses wherein the first transistor and the second transistor are identical in conductivity, *e.g.*, they can both be p-channel or n-channel transistors (*see* Koyama, ¶¶ [0113]-[0118] and [0148]-[0152]).

As to claim 43, 50 and 58, Koyama discloses wherein the light-emitting device (or element substrate) is incorporated into at least one selected from the group consisting of a cellular phone, a mobile computer, a game machine, an electronic book, a video camera, a digital camera, a goggle display, a display device, and a navigation system (*see* Koyama, ¶ [0002]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 41, 42, 44, 45, 48, 49, 51-54, 56, 57, 59 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2001/0002703 by Koyama.

As to claims 41, 42, 48, 49, 56 and 57, Koyama discloses the first transistor and second transistor having a channel length and a channel width, *e.g.*, implicitly suggested in thin film transistors. However, Koyama does not disclose expressly wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal to or shorter than a channel width, wherein a ratio of the channel length to the channel width of the first transistor is 5

more, as claimed. At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the first transistor and second transistor had channel widths/lengths as claimed because applicant has not disclosed that such a specific transistor channel length/width provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor channel width/length because both would perform equally well in functioning as switches in a pixel of a display device.

As to claims 44, 51 and 59, Koyama discloses wherein the signal line (*see* Koyama, 107; Fig. 3), the first power line (*see* Koyama, 110; Fig. 3), and the second power line (*see* Koyama, 113; Fig. 3) are provided in parallel with each other (*see* Koyama, ¶ [0115]). Although Koyama does not disclose expressly the order of these three lines per pixel, there are three possibilities: 1) the first power line is provided between the signal line and the second power line; 2) the second power line is provided between the signal line and the first power line; and 3) the signal line is provided between the first power line and the second power line. Thus, Koyama does not disclose expressly wherein the first power line is provided between the signal line and the second power line, as claimed.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify Koyama such that the first power line is provided between the signal line and the second power line because applicant has not disclosed that such a specific configuration provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with having the signal line, first power line, and second power line in parallel with one another in a different order, *e.g.*, any one of those suggested

by Koyama, because both would perform equally well at providing the predictable result of in driving the various transistors in a pixel of a display device.

As to claims 45, 52 and 60, Koyama discloses wherein the second power line (see Koyama, 113; Fig. 3) has an electric potential so that the first transistor (see Koyama, 112; Fig. 3) operates in an on-state when the second transistor (see Koyama, 109; Fig. 3) is in an on-state (see Koyama, ¶¶ [0132] and [0139]). However, Koyama does not disclose expressly wherein the first transistor is in a *saturation region* when the second transistor is in an on-state, as claimed.

Examiner respectfully submits that it is old and well-known to operate thin film transistors in a saturation region when in an on-state, particularly in the application of a switching device. Thus, it would have been obvious to one having ordinary skill in the art to further modify the light-emitting device of Koyama such that the first transistor is in a saturation region when in an on-state. The suggestion/motivation for doing so would have been because, as one of ordinary skill in the art would appreciate, a thin film transistor acting as a switch and operating in a saturation region provides predictable and stable operation characteristics when using analog values as in the embodiment of Koyama.

As to claim 53, Koyama discloses wherein each of the first transistor and the second transistor has P-type conductivity (see Koyama, ¶¶ [0150]-[0152]) wherein each transistor has a threshold value, *e.g.*, implicitly suggested in a transistor. However, Koyama does not disclose wherein a threshold value of the first transistor is higher than that of the second transistor, as claimed. At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the threshold value of the first transistor is higher than that of the second transistor as claimed because applicant has not disclosed that such a specific threshold value relationship provides an advantage, is used for a particular purpose, or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor threshold value relationship for a pixel in a display device because both would perform equally well in functioning as switches in a pixel of a display device.

As to claim 54, Koyama discloses wherein each of the first transistor and the second transistor has an N-type conductivity (Koyama, ¶¶ [0150]-[0152]) wherein each transistor has a threshold value, *e.g.*, implicitly suggested in a transistor. However, Koyama does not disclose expressly wherein a threshold value of the first transistor is lower than that of the second transistor, as claimed. At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the teachings of Koyama such that the threshold value of the first transistor is lower than that of the second transistor as claimed because applicant has not disclosed that such a specific threshold value relationship provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with any commercially available transistor threshold value relationship for a pixel in a display device because both would perform equally well in functioning as switches in a pixel of a display device.

7. Claims 40, 47 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2001/0002703 by Koyama in view of U.S. Patent No. 6,207,969 to Yamazaki ("Yamazaki").

As to claims 40, 47 and 55, Koyama does not disclose expressly wherein the first transistor is a depletion type transistor, as claimed. Yamazaki discloses a light-emitting device comprising a depletion type transistor for driving a light-emitting element (*see* Koyama, Figs. 1-2B, 14; *see also* col. 1, ll. 13-15 and 46-53). At the time the invention was made, it would have been obvious to one having ordinary skill in the art to further modify the teachings of Koyama such that the first

transistor is a depletion type transistor, as taught by Yamazaki. The suggestion/motivation for doing so would have been so that the transistor could be formed on a single crystal silicon film by an intrinsic semiconductor in a silicon on insulator (*see* Yamazaki, col. 1, ll. 45-53), as one of ordinary skill in the art would appreciate.

8. Claims 3, 15, 19, 25, 28, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2001/0002703 by Koyama in view of U.S. Patent No. 7,209,101 to Abe ("Abe").

As to claim 3, most of the claim limitations have been addressed in the discussion of claim 36 above, with the exception of: a fourth transistor for forcing the light-emitting element into a non-emission state irrelevant from the video signal, as claimed. Koyama does not disclose expressly this limitation.

Abe discloses a pixel (*see* Abe, 2; Figs. 8 and 33) for a light-emitting device, analogous in art with Koyama, comprising at least four switches, wherein a fourth switch (*see* Abe, SW4) is provided for forcing a light-emitting element (*see* Abe, LED) of the pixel into a non-emission state irrelevant from the video signal (*see* Abe, col. 12, ll. 18-42; *see also* col. 21, l. 53 - col. 22, l. 4). At the time the invention was made it would have been obvious to one having ordinary skill in the art to modify the light-emitting device of Koyama such that the pixel comprised a fourth switch for forcing the light-emitting element into a non-emission state irrelevant from the video signal, as taught by Abe. As one of ordinary skill in the art would appreciate, the suggestion/motivation for doing so would have been to forcibly remove any charges stored in the light-emitting element, thereby stopping light emission by the light-emitting element simultaneously with stopping the supply of the current thereto, so that the light emission period of the light-emitting element can be controlled with higher precision (*see* Abe, col. 12, ll. 29-35; *see also* col. 22, ll. 1-4).

Although Abe does not disclose expressly wherein the fourth switch is a *transistor*, as claimed, examiner takes Official Notice that the use of transistors as switching elements in display pixels is old and well-known in the art. Thus, at the time the invention was made it would have been obvious to one having ordinary skill in the art to further modify the light-emitting device of Koyama and Abe such that the fourth switch is a transistor. As one of ordinary skill in the art would appreciate, the suggestion/motivation for doing so would have been to facilitate a manufacturing process of the light-emitting device by using old, well-known and readily accessible devices as switches. Furthermore, because both teachings control transmission of a signal via a control signal, it would have been obvious to one having ordinary skill in the art to substitute one means for the other to achieve the predictable result of functioning as a switch.

As to claims 15, 19, 25, 28, 34 and 35, these limitations have been addressed in the discussion of claims 39 and 41-45, respectively.

As to claim 32, Koyama discloses wherein the electric potential of the second power line is fixed (*see* Koyama, ¶ [0139]).

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2001/0002703 by Koyama in view of U.S. Patent No. 7,209,101 to Abe as applied to claims 3, 15, 19, 25, 28, 32, 34 and 35 above, and further in view of U.S. Patent No. 6,207,969 to Yamazaki.

As to claim 17, Koyama is modified by Yamazaki in the same manner and for the same reasons set forth in the discussion of claims 40, 47 and 55 above. Thus, examiner respectfully submits that these limitations have already been addressed.

Response to Arguments

10. Applicant's arguments filed November 2, 2009, have been fully considered but they are not persuasive.

Applicant argues that Koyama does not teach or suggest that “**a source of the first transistor is connected to the first power line** and a gate electrode of the first transistor is connected to a second power line so that a voltage between the gate electrode and the source of the first transistor is constantly fixed,” as recited in independent claim 3 (emphasis added). Instead, applicant argues that one of the source or the drain terminals of the transistor 112 is connected to the electroluminescent element 111, and the other drain or source of the transistor is connected to a source or drain terminal of another transistor 109 (Amend., p. 11).

Examiner respectfully disagrees and submits that Figure 3 of Koyama illustrates that the other drain or source of the first transistor 112 is connected to the first power line 110 **through another transistor 109**, thus reading on the claim limitation argued above. Furthermore, examiner respectfully submits that the claims presented are absent any language that would preclude such an interpretation.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571)272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander S. Beck/
Primary Examiner, Art Unit 2629

Dated: January 18, 2010